

SYLLABUS

ECE 327: Digital Computer Design 3(3,0) Section 1 - Spring Semester, 2005

- Goals:** Understand design of high-speed ALUs
Understand design of control and timing circuitry
Understand modern design methodologies (CAD and HDL)
Understand design for FPGA devices
- Instructor:** Walt Ligon, 656-1224, 300-D Riggs Hall,
walt@clemson.edu
- Office Hours:** MW 3:30 to 5:00 or by appointment
- Text:
Required:** *Fundamentals of Digital Logic with Verilog Design*
By: Stephen Brown and Zvonko Vranesic,
McGraw Hill ISBN: 0-07-282315-1
Recommend a good Verilog text such as
Starter's Guide to Verilog 2001
by Ciletti Prentice Hall ISBN: 0-13-141556-5
- Grading:** Mid-Term Exam: 20%
2nd Exam: 20%
Assignments and Projects: 40%
Final Exam: 20%
- Attendance:** Attendance is required
No late work accepted.
Make-up tests by prior appointment only.
Wait 15 minutes for late instructor.
- Academic Honesty:** All work on quizzes, tests, exams, design assignments, projects,
and labs is to be wholly your own. Possessing, using, providing, or
exchanging improperly acquired written, verbal, or electronic
information will be considered a violation of the academic honor
code. Violations will result in a grade of F for the semester.

ECE327 - Topic List

- Introduction to CAD tools and simulation
 1. CAD workflow
 2. Technologies (ASIC, programmable logic, discrete logic)
 3. Logic vs. electrical simulation
 4. Time vs. event simulation
 5. Special problems in simulation
 6. Schematic capture vs. HDLs
- Verilog Introduction (1 week)
 1. Modules, gates
 2. Signals, nets, variables
 3. Concurrent statements
 4. Always and initial
 5. Testbenches
- Synchronous Sequential Design (5 weeks)
 - State Machines
 1. More and Mealy Models
 2. Algorithmic state machines
 3. Regular language recognizers
 4. Verilog specification
 - Register Transfer Level Design
 - ALU Design
 1. Shift-add multipliers
 2. Bit-pair recoding
 3. General arithmetic logic units
 - Design for FPGAs
- Asynchronous Sequential Design (2 weeks)
 1. Fundamental mode circuit analysis
 2. Synthesis from flow tables
 3. Asynchronous state diagram and primitive flow tables
 4. State reduction
 5. State assignment
 6. Races and hazards
 7. Verilog specification
- Floating Point (2 weeks)
 1. Formats
 2. Addition/Subtraction
 3. Multiplication
 4. Hardware organization
 5. Rounding, special values
- Logic Minimization (1 week)
 1. Quine-McClusky tabular method
- Circuit Testing (1 week)

Academic Honesty: All work on quizzes, tests, design assignments, and labs is to be wholly your own. Possessing, using, providing, or exchanging improperly acquired written, verbal, or electronic information will be considered a violation of the academic honest policy. Violations will result in a grade of F for the semester.

Examples of academic honest violations include, but are not limited to:

- Possessing, using, or exchanging similar projects from previous semesters
- Collaborating on individual assignments
- Multiple groups collaborating on group projects

I have read and understood the above stated academic honesty policy. I accept that any form of academic dishonesty, as described above, will result in a minimum punishment of a grade of F in the course.

Name

Signed

Date