

ECE327 - Study Guide 1 & 2

- Introduction to CAD tools and simulation (Notes)
 - CAD workflow (Chapter 1, 2.9, 2.10)
 - Design entry
 - netlist, EDIF
 - Device library
 - Logic simulation
 - Place and Route
 - Timing simulation
 - Back annotation
 - Technologies (ASIC, PAL, PLA, FPGA, discrete logic) (3.5, 3.6, 3.7)
 - Simulation
 - Logic vs. electrical simulation
 - Time vs. event simulation
 - Switch-level simulation
 - Mixed-mode simulation
 - Rise (fall) time versus rise (fall) delay
 - Special problems in simulation
 - Tri-state buffers (TSBs) and transmission gates (TGs)
 - Competing driving strength
 - Charge storage, charge decay, charge sharing
 - Multi-valued logic
 - Schematic capture vs. HDLs
 - Behavioral vs structural modeling
 - Hierarchical modeling
- Verilog Introduction (Appendix A, sections 1 - 11, 14, 15, Notes)
 - Modules, gates
 - Signals, nets, variables, wires, registers
 - Concurrent assignment statements
 - Always and initial
 - Testbenches
 - unit under test
 - time management statements (#, @, wait)
 - Combinational Logic
 - Flip-flops
 - Registers (simple, shift, counters, etc.)
 - State machines
- Synchronous Sequential Design (Chapter 8)
 - State Machines
 - More and Mealy Models (8.1, 8.3)
 - Algorithmic state machine (8.10)
 - Register Transfer Level Design
 - State encoding (8.2)
 - gray code encoding
 - one-hot encoding
 - Regular language recognizers

- Counters (8.7)
- State minimization (8.6)
- ALU Design
 - Shift-add multipliers (10.2.3)
 - Booth recoding
 - Bit-pair recoding
 - Array multipliers (5.6)

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- Floating Point Units
 - Formats
 - sign/magnitude
 - excess or biased notation
 - normalized mantissa
 - Floating point arithmetic
 - Multiplication
 - Addition/Subtraction
 - Hardware organization
 - Control logic
 - Programmable Logic Devices
 - ROMs
 - mask programmable
 - programmable (PROM)
 - erasable/programmable (EPROM)
 - electrically erasable (EEPROM)
 - PLAs
 - PALs
 - CPLDs
 - FPGAs
 - MUX based
 - LUT based
 - reprogrammable (SRAM)
 - partially reprogrammable
 - components
 - configurable logic block (CLB)
 - IO logic block
 - switching matrix
 - routing resources
 - single, double, quad, long lines
 - Xilinx Spartan
 - Xilinx Virtex
 - Implementation technologies
 - MOS transistor structure
 - simple switching circuits
 - CMOS complementary switching circuits
 - CMOS switching characteristics
 - Transmission gates and TSBs
 - Array logic implementation

- Asynchronous Sequential State Machines
 - Fundamental mode circuits
 - Flow tables
 - Asynchronous state diagram
 - Primitive flow table
 - Implication table
 - Compatible pairs
 - Dependencies
 - Merger digram
 - Maximal compatibles
 - Dependencies
 - Closed cover
 - Race-free state assignment
 - critical and non-critical races
 - transition diagram
 - “add a row” method
 - multiple row method
 - Hazards
 - static hazards
 - dynamic hazards
 - removing hazards
- Tabular Method for Logic Minimization
 - Finding prime implicants with lists
 - Selecting a minimum cover
 - essential prime implicants
 - row dominance
 - column dominance
 - branching
 - Using “don't cares”
 - Multiple functions