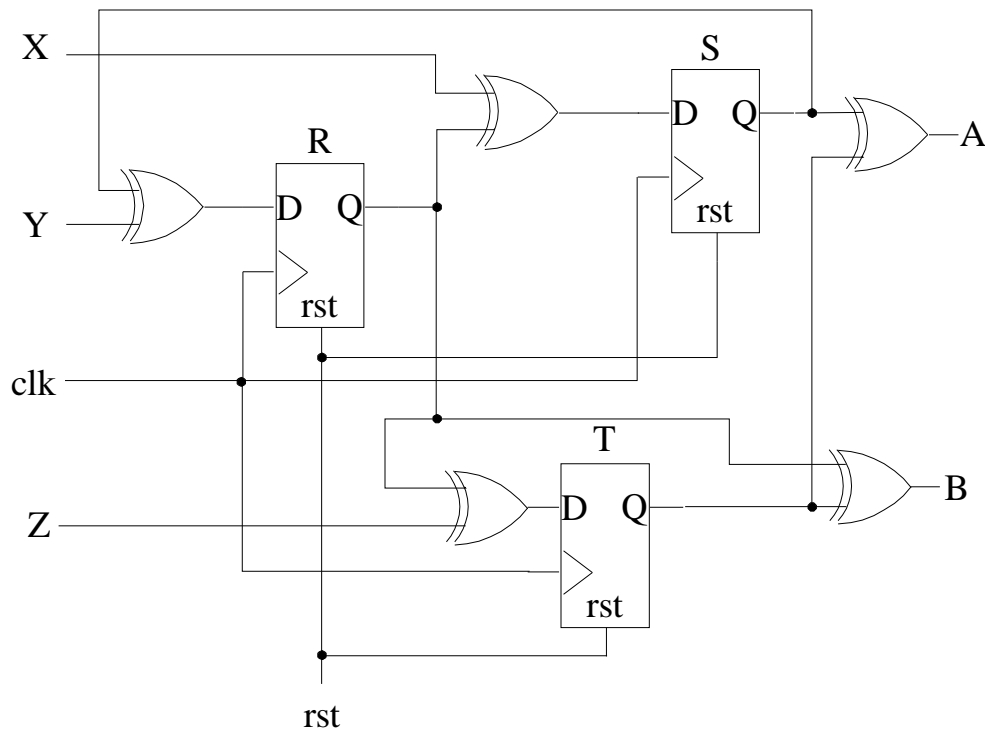


**ECE 327 Spring 2005**  
**Assignment 2 - Due 02/02/05**  
**Simulate a Simple Sequential Circuit with Verilog**

Design a circuit with the following interface:

```
module assign2 (clk, rst, x, y, z, A, B );
    input clk, rst, x, y, z;
    output A, B;
endmodule
```

and the following implementation:



**What to turn in:** Write a report with an introduction, including motivation, and circuit diagram, a listing of the Verilog code, and simulation outputs showing correct operation. The simulation outputs must be annotated to demonstrate that the output is correct.

There are 64 possible tests for this circuit. You should try to run as many of them as possible. Some may not be possible.