

NAME _____

ECE 327 Test 1 Fall 2003

1) Term matching. Write the number of the best term for each definition. Not all terms must be used. Some may be used twice.

- | | |
|----------------------------|----------------------------|
| 1. ASIC | 17.place and route |
| 2. FPGA | 18.back annotation |
| 3. discrete logic | 19.module |
| 4. schematic capture | 20.always |
| 5. HDL | 21.initial |
| 6. electrical simulation | 22.continuous assignment |
| 7. logical simulation | 23.non-blocking assignment |
| 8. time-based simulation | 24.behavioral |
| 9. event-based simulation | 25.structural |
| 10.switch-based simulation | 26.Moore model |
| 11.netlist | 27.Mealy model |
| 12.EDIF | 28.synthesis |
| 13.multi-valued logic | 29.state assignment |
| 14.tri-state buffer | 30.one-hot encoding |
| 15.rise(fall) time | 31.unit under test |
| 16.rise(fall) delay | 32.testbench |

___a) A state machine model that has outputs associated only with the current state value.

___b) An HDL assignment that re-evaluates any time one of its inputs changes.

___c) A simulation method where node values are recomputed only when their inputs change.

___d) The process of modifying simulation parameters such as delay values based on the results of place and route.

___e) A standardized data structure for representing a circuit by listing the circuit components and the interconnections between them.

NAME _____

ECE 327 Test 1 Fall 2003

2) True/False. For each statement, indicate whether the statement is true (T) or false (F). If a statement is not necessarily true, you should indicate false (F).

___a) ASICs are the fastest and densest technology for digital circuits.

___b) The Moore model is clearly superior in all ways to the Mealy model and is the only approach that is reasonable for designing state machines.

___c) In Verilog you can use the blocking or non-blocking assignment interchangeably. The difference is only in how fast your simulation runs.

___d) HDLs allow both structural and behavioral implementations of a design unit, and in fact can combine the two techniques.

___e) One-hot encoding is often a good state assignment scheme because it simplifies state decoding and is easy to understand.

NAME _____

ECE 327 Test 1 Fall 2003

3) State Machine Design

Design a state machine that outputs a 1 if the previous three inputs are alternating 1's and 0's. Use a Moore model.

Example:

input: 1 1 1 0 1 0 1 0 1 1 0 1 0 0 1 0 1 0 1 0 1 0 1 1 1 ...
output: 0 0 0 0 0 1 1 1 1 1 0 0 1 1 0 0 1 1 1 1 1 1 1 1 0 ...

Draw a state diagram for the state machine.

NAME _____

ECE 327 Test 1 Fall 2003

4) Verilog

Write a Verilog module to behaviorally implement a rising-edge triggered 16 bit register with an asynchronous active-high reset and two control signals. When the control signal "load" is high, load the register from the parallel input "din." When the control signal "flip" is high and the control signal "load" is not high, swap the least significant byte of the current register contents with the most significant byte of the current register contents. The interface is given below:

```
module flipreg (clk, rst, load, flip, din, dout);  
  
input clk, rst, load, flip;  
input [15:0]din;  
output [15:0]dout;
```