SYLLABUS

ECE 327: Digital Computer Design 3(3,0)
Section 1 – Fall Semester, 2002

Goals:
Understand design of high-speed ALUs
Understand design of control and timing circuitry
Understand modern design methodologies (CAD and HDL)
Understand design for FPGA devices

Instructor: Walt Ligon, 656–1224, 300–D Riggs Hall,
walt@clemson.edu

Office Hours: MW 3:30 to 5:00 or by appointment

Text:
Required: Digital Logic Circuit Analysis and Design
By: Victor P. Nelson, H. Troy Nagle, Bill D. Carroll, and J. David Irwin
ISBN: 0134638948

VHDL Starter’s Guide
By: Sudhakar Yalamanchili
1998, Prentice Hall

Suggested: The Designer’s Guide to VHDL
By: Peter J. Ashenden
1996, Morgan Kauffman

HDL Chip Design
By: Douglas J. Smith
1996, Doone Publications

Grading:
Mid-Term Exam: 25%
Assignments and Projects: 50%
Final Exam: 25%

Attendance: No late work accepted.
Make-up tests by prior appointment only.
Wait 15 minutes for late instructor.
**Academic Honesty:** All work on quizzes, tests, design assignments, and labs is to be wholly your own. Possessing, using, providing, or exchanging improperly acquired written, verbal, or electronic information will be considered a violation of the academic honor code. Violations will result in a grade of F for the semester.

**ECE327 – Topic List**

- VHDL Introduction (1 week)
  1. Entities, architectures, configurations
  2. Signals and signal assignments
  3. Processes, statements, wait for, after
  4. Components and instantiation
  5. Testbenches
- Asynchronous Sequential Design (2 weeks)
  1. Fundamental mode circuit analysis
  2. Synthesis from flow tables
  3. Asynchronous state diagram and primitive flow tables
  4. State reduction
  5. State assignment
  6. Races and hazards
  7. VHDL specification
- Synchronous Sequential Design (5 weeks)
  - State Machines
    1. More and Mealy Models
    2. Algorithmic state machines
    3. Regular language recognizers
    4. VHDL specification
  - Register Transfer Level Design
  - ALU Design
    1. Shift–add multipliers
    2. Bit–pair recoding
    3. General arithmetic logic units
  - Design for FPGAs
- Floating Point (2 weeks)
  1. Formats
  2. Addition/Subtraction
  3. Multiplication
  4. Hardware organization
  5. Rounding, special values
- Logic Minimization (1 week)
  1. Quine–McClusky tabular method
- Optimal State Assignment (2 weeks)
- Circuit Testing (1 week)
Academic Honesty: All work on quizzes, tests, design assignments, and labs is to be wholly your own. Possessing, using, providing, or exchanging improperly acquired written, verbal, or electronic information will be considered a violation of the academic honest policy. Violations will result in a grade of F for the semester.

Examples of academic honest violations include, but are not limited to:

– Possessing, using, or exchanging similar projects from previous semesters
– Collaborating on individual assignments
– Multiple groups collaborating on group projects

I have read and understood the above stated academic honesty policy. I accept that any form of academic dishonesty, as described above, will result in a minimum punishment of a grade of F in the course.

________________________________________
Name

_________________________________________
Signed Date